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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/047,344	01/15/2002	Kang Wu	10010958-1	5090

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EXAMINER	
ABRAHAM, ESAW T	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/047,344	WU ET AL.	
	Examiner	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/04/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **1-13** are presented for examination.

Information Disclosure Statement

2. The applicant's IDS of August 04 20003 has been entered. The examiner considers the IDS.

Claim objections

3. Claims **1 and 11-13** are objected to because of the following informalities:

(a) Please change the phrase "A method for the elimination of" to "A method for eliminating" (see page 14, line 2 of claim 1) and change the phrase "the reordering of" to "reordering" (see page 14, line 2 of claim 1).

(b) Please change the phrase "A method for the reordering" to "A method for reordering" (see page 16, line 10 of claim 11)

(c) Please change the phrase "the execution" to "an execution" (see page 16 line 11 of claim 11).

(d) Please change the phrase "A method for the elimination of" to "A method for eliminating" and remove the word "the" before the word "reordering" (see page 17, line 22 or claim 12).

(e) Please change the phrase "A method for the reordering" to "A method for reordering" (see page 17, line 23 of claim 12).

(f) Please change the phrase "the execution" to "an execution" (see page 17 line 24 of claim 12).

(h) Please change the phrase "A method for the reordering" to "A method for reordering" (see page 19, line 5 of claim 13).

(i) Please change the phrase "the execution" to "an execution" (see page 19 line 6 of claim 13).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U. S. C 112

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 9, recites the limitation "the optimized set" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101, Non Statutory

5. Claims **1-13** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter because:

a) The language of the claims 1 and 11-13 raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment or machine or manipulates abstract idea or solves a purely mathematical problem without any limitation to a practical application which would result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C 101.

Claims **2-10,** which are dependents of claim 1 are also rejected under 35 U.S.C 101.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saw et al. (5,345,450).

As per claims **1 and 11-13,** Saw et al. in figure 7 teach a flow chart of a method utilized for reducing the simulation time and data storage requirements for a computer simulation of a logic device, where the simulation involves a series of redundant input and expected output vectors (see col. 5, lines 43-48). Saw et al. in step 1040, teach a reduced set of input vectors is generated for simulation from the sequence of input vectors selected in step (1010), by eliminating all but the first of the redundant input vectors in the series of redundant input vectors having the same expected output vectors (see col. 6, lines 38-52), in step (1060), the reduced set of input vectors are then provided to a computer simulation (e.g., 100 in FIG. 8A) of the logic device 10 along with the associated control bits (e.g., CB1 and CB2) of each input vector, as schematically

illustrated in FIG. 8A, in order to generate the corresponding expected output vectors for each of those input vectors. Saw et al. **do not explicitly** teach or use the same terminologies of representing sequences of tests as a correlation vector, calculating a product of each correlation vector and the vector and updating the vector. **However,** Saw et al. in figure 7, step 1070 teach a set of test vectors formed by combining each input vector of the reduced set of input vectors, including its associated control bits, with its corresponding output vector resulting from the computer simulation (see col. 7, lines 3-21) and further Saw et al. in step 1090 teach that the reduced set of input vectors expanded by a post processor (e.g., 150 in FIG. 9A) according to the information contained in the encoded control bits to either form the original sequence of input vectors or some modified sequence of input vectors which Saw is basically teaching the same method of as the applicant's claim. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to follow the steps or the flow chart of Saw et al. to correlate and update vectors. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would be relatively and yet high to minimize the time for testing and the processing power or resource consumption.

As per claims **2 and 3,** Saw et al. teach all the subject matter claimed in claim 1 including Saw et al. in figure 7, step 1070 teach a set of test vectors formed by combining (correlating) each input vector of the reduced set of input vectors, including its associated control bits, with its corresponding output vector resulting from the computer simulation (see col. 7, lines 3-21).

As per claim **4,** Saw et al. teach all the subject matter claimed in claim 1 including Saw et al. teach that a test program generating step comprises the step of changing said finite duration

to a longer period equal to said minimum period multiplied by the number of redundant input vectors in said series of redundant input vectors and divided by the number of times said first input vector is duplicated (see claim 7).

As per claims **5 and 6,** Saw et al. teach all the subject matter claimed in claim 1 including Saw et al. teach output values being detected across the outputs 30 are not expected to change during this programming period, 25,000 redundant test vectors comprising the 25,000 redundant input and 25,000 redundant output vectors will be executed by the logic device tester 50 (see col. 4, last paragraph).

As per claims **7-10,** Saw et al. teach all the subject matter claimed in claim 1 including Saw et al. in figure 7, step 1070 teach a set of test vectors formed by combining (correlating) each input vector of the reduced set of input vectors, including its associated control bits, with its corresponding output vector resulting from the computer simulation (see col. 7, lines 3-21).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,256,593 Damon et al.

US PN: 6,810,372 Unnikrishnan et al.

US PN: 6,782,501 Distler et al.

8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100